Novel Method for Determination of Junction-FET Access Resistances

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Abstract— **A new method for extracting JFET access resistances, which does not need to consider the intrinsic channel resistance of the device, is presented. The method uses an impedance data set measured over a range of bias points. The data set is reduced to those points with reciprocal impedance matrices and appropriate bias conditions. The extraction procedure is ideal for automated device characterisation.**

Introduction

TRANSISTOR access resistances impose a fundamental limit on performance. Connection to the drain, gate and source terminals of the intrinsic device must be made through these resistances, which limit optimum noise, distortion, gain and frequency performance. Correct determination of the access resistances is therefore critical for accurate modeling of the behavior of devices and circuits.

MESFET access resistances can be determined from dc measurements. A popular procedure is to recursively fit the measured drain-to-source resistance, at zero drain potential, to a dimensionless function of gate-source bias [1]. The dimensionless function is based on the uniform channel approximation and requires the barrier potential of the MESFET's Schottky junction, which is estimated from measurement.

Impedance parameters, obtained from ac scattering parameter measurements, can also be used to determine the access resistances [2]. A uniformly distributed intrinsic channel resistance is assumed and total channel resistance, determined from drain-source resistance measurements, must be known [3]. Similar techniques are the basis for extraction of small-signal device models [4], [5].

These extraction procedures use *a priori* knowledge of certain device technology parameters. The determination of these parameters, however, is influenced by the access resistances. A technique that does not require knowledge of the intrinsic channel behavior is needed to ameliorate this *chicken-and-the-egg* dilemma. In practice, the device is measured in common-source configuration with zero drain-source bias (cold-fet condition) and a simple distributed model of the channel is assumed. Extraction is more accurate if the device is a reciprocal linear two-port system. When the device is reciprocal, the channel behavior can be isolated from the extraction procedure. As shown in this paper, this condition occurs at non-zero drain-source biases.

Proposed here is an alternative procedure based on measured dc impedance parameters at operating points where the device exhibits reciprocity. Very little is assumed about the intrinsic device. No knowledge of intrinsic channel resistance is required. The sole assumption made is that the gate current results from conduction through a gate-channel Schottky junction.

The proposed technique has been implemented to use an arbitrary array of current-voltage data measured over both positive and negative drain-source biases. It is ideal for an automated characterization system and, when used in conjunction with fast measurement equipment [6], is suitable for on-the-fly production testing.

Intrinsic Impedances

The new extraction procedure is developed by describing behavior of the intrinsic device as a linear two-port system. Two-port conductance parameters, g_{ij}, describe small-signal gate and drain currents, i_g and i_d, in terms of gate and drain potentials, v_{gs} and v_{ds},

$$\begin{pmatrix} i_g \\ i_d \end{pmatrix} = \begin{pmatrix} g_{11} & g_{12} \\ g_{21} & g_{22} \end{pmatrix} \begin{pmatrix} v_{gs} \\ v_{ds} \end{pmatrix} \tag{1}$$

and impedance parameters, z_{ij}, describe the small-signal potentials in terms of the currents.

$$\begin{pmatrix} v_{gs} \\ v_{ds} \end{pmatrix} = \begin{pmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{pmatrix} \begin{pmatrix} i_g \\ i_d \end{pmatrix} \tag{2}$$

The impedance matrix is the inverse of the conductance matrix.

$$\begin{pmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{pmatrix} = \frac{1}{g_{11}g_{22} - g_{12}g_{21}} \begin{pmatrix} g_{22} & -g_{12} \\ -g_{21} & g_{11} \end{pmatrix} \tag{3}$$

If the system is reciprocal then $z_{12} = z_{21}$ and $g_{12} = g_{21}$, and gate terminal, drain terminal, and source terminal impedance equations respectively can be established from (3) as:

$$z_{11} - z_x = \frac{g_{22} + g_x}{g_{11}g_{22} - g_x^2} \tag{4}$$

$$z_{22} - z_x = \frac{g_{11} + g_x}{g_{11}g_{22} - g_x^2} \tag{5}$$

and

$$z_x = \frac{-g_x}{g_{11}g_{22} - g_x^2} \tag{6}$$

where $z_x = z_{12} = z_{21}$ and $g_x = g_{12} = g_{21}$.

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The intrinsic gate, drain, and source terminals are connected to extrinsic access resistances R_G, R_D, and R_S respectively. These resistances contribute to the extrinsic small-signal impedance matrix, which can be easily measured.

$$\begin{pmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{pmatrix} = \begin{pmatrix} z_{11} + R_S + R_G & z_{12} + R_S \\ z_{21} + R_S & z_{22} + R_S + R_D \end{pmatrix} \tag{7}$$

If the gate junction is a Schottky barrier then the above equations form the basis for extracting the three access resistances from extrinsic impedance matrices measured at several bias points.

Terminal Impedances

Gate current results from conduction through the gate-channel Schottky junction. A portion of this current will be from gate to source and the remainder from gate to drain.

When the large-signal current from gate to drain is dominant, the gate current can be described by

$$I_G \approx I_o e^{V_{GD}/V_T} \tag{8}$$

This can be assumed to be the case when $V_{GS} \gg V_T$ and $V_{DS} \ll -V_T$ ($V_T = q/nkT$), and when the current exiting the drain is approximately equal the gate current. That is, when $I_S \approx 0$ because $I_S = -(I_D + I_G)$.

Alternatively, the large-signal current from gate to source may dominant and gate current is then described by

$$I_G \approx I_o e^{V_{GS}/V_T} \tag{9}$$

This can be assumed to be the case when $V_{GS} \gg V_T$ and $V_{DS} \gg +V_T$, and when $I_D \approx 0$.

Gate Terminal

If $I_S \approx 0$, and $V_{GS} \gg V_T$ and $V_{DS} \ll -V_T$, then the gate-terminal conductance parameters, determined from (8), are

$$g_{11} = \frac{\partial I_G}{\partial V_{GS}} = \frac{I_G}{V_T} \tag{10}$$

and

$$g_{12} = \frac{\partial I_G}{\partial V_{DS}} = \frac{-I_G}{V_T} \tag{11}$$

Substitution of (10) and (11) into (4) gives the intrinsic gate-terminal impedance equation in terms of gate current.

$$z_{11} - z_x = \frac{V_T}{I_G} \tag{12}$$

This equation is also derived from (9) when $I_D \approx 0$, and $V_{GS} \gg V_T$ and $V_{DS} \gg +V_T$.

Drain Terminal

Again, if $I_S \approx 0$, and $V_{GS} \gg V_T$ and $V_{DS} \ll -V_T$, then gate-to-drain conduction dominates. The drain-terminal conductance parameters, from (8), become

$$g_{22} = \frac{\partial I_D}{\partial V_{DS}} \approx \frac{\partial(-I_G)}{\partial V_{DS}} = \frac{I_G}{V_T} \tag{13}$$

and

$$g_{21} = \frac{\partial I_D}{\partial V_{GS}} \approx \frac{\partial(-I_G)}{\partial V_{GS}} = \frac{-I_G}{V_T} \tag{14}$$

Substitution of (13) and (14) into (5) gives the intrinsic drain-terminal parameter in terms of gate or drain current.

$$z_{22} - z_x \approx \frac{V_T}{I_G} \approx -\frac{V_T}{I_D} \tag{15}$$

Source Terminal

If $I_D \approx 0$ and $V_{DS} \gg +V_T$, the source terminal conductance parameters, defined in terms of I_S, become

$$-\frac{\partial I_S}{\partial V_{DS}} = \frac{\partial I_D}{\partial V_{DS}} + \frac{\partial I_G}{\partial V_{DS}} = g_{22} + g_{12} \approx 0 \tag{16}$$

and

$$-\frac{\partial I_S}{\partial V_{GS}} = \frac{\partial I_D}{\partial V_{GS}} + \frac{\partial I_G}{\partial V_{GS}} = g_{21} + g_{11} = -\frac{I_S}{V_T} \tag{17}$$

Substitution of (16) for g_{22} and (17) for $(g_{11} + g_x)$ in (6) gives the intrinsic source-terminal impedance equation in terms of gate and drain current (noting that $g_x = g_{12} = g_{21}$).

$$z_x = -\frac{V_T}{I_S} = \frac{V_T}{I_G + I_D} \tag{18}$$

Extraction of Access Resistances

The proposed procedure extracts the access resistances from extrinsic impedance matrices measured over a range of bias points. The measurements are sorted to produce data sets that satisfy the conditions required for the three impedance relationships (12), (15), and (18).

The first step in the procedure is to discard all impedance data for which $|Z_{12} - Z_{21}|$ is less than a specified *reciprocal tolerance* value. That is, only impedance matrices for which $Z_{12} \approx Z_{21}$ are used for the extraction. Figure 1 shows a typical reduction of the data set using three reciprocal tolerances.

Gate Resistance

The second step is to isolate data for which $V_{GS} \gg V_T$ and $V_{DS} \ll -V_T$, which is the condition required for (12). Substitution of (7) for $z_{11} - z_x$ gives the following relationship:

$$Z_{11} - Z_x = \frac{V_T}{I_G} + R_G \tag{19}$$

A plot of $Z_{11} - Z_x$ as a function of inverse gate current has slope V_T and intercept R_G. Figure 2 shows that this plot approaches a straight line when the data set consists of only those points where $I_S \approx 0$. The line of best fit gives $V_T = 31.41$ mV and $R_G = 0.652\ \Omega$.

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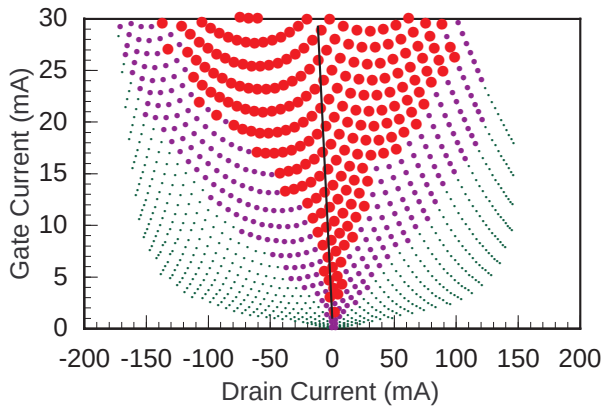

Fig. 1. Measured current from a typical MESFET. The dot size indicates the tolerance of reciprocity at each point, from $|z_{12} - z_{21}|$ being less than 5.0 Ω (small dots), or less than 0.5 Ω (medium dots), to less than 0.1 Ω (large dots). The almost vertical line is the locus of $V_{DS} = 0$.

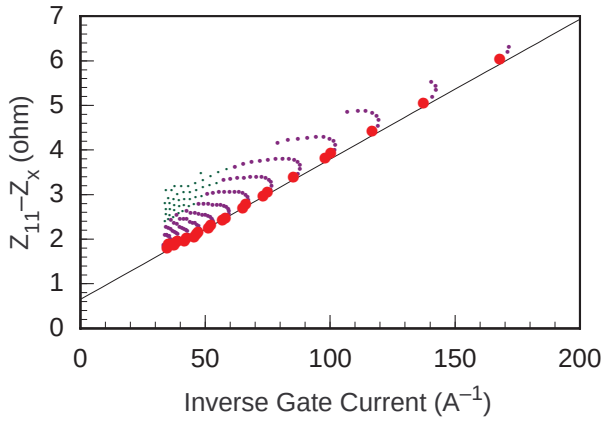

Fig. 2. A plot of gate-terminal impedance (19) from reduced sets of data with a reciprocal tolerance of 0.5 Ω, $V_{DS} < -0.1$ V. The large dots indicate $|I_S| < 20$ mA, and the medium dots indicate $|I_S| < 100$ mA, and small dots indicate no current restriction. The line is a least square fit to the large dots.

Drain Resistance

The third step is to isolate data for which $V_{GS} \gg V_T$ and $V_{DS} \ll -V_T$, and $I_S \approx 0$ which is the condition required for (15). Substitution of (7) for $z_{22} - z_x$ gives the following relationship:

$$Z_{22} - Z_x = -\frac{V_T}{I_D} + R_D \tag{20}$$

A plot of $Z_{22} - Z_x$ as a function of inverse drain current has slope $-V_T$ and intercept R_D. Figure 3 shows that this plot approaches a straight line when the data set is reduced to those points for which $V_{DS} \ll -V_T$. The line of best fit gives $V_T = 31.46$ mV and $R_D = 1.09$ Ω

Source Resistance

The final step is to isolate data for which $V_{GS} \gg V_T$ and $V_{DS} \gg +V_T$, and $I_D \approx 0$ which is the condition required for (18). Substitution of (7) for z_x gives the following relationship:

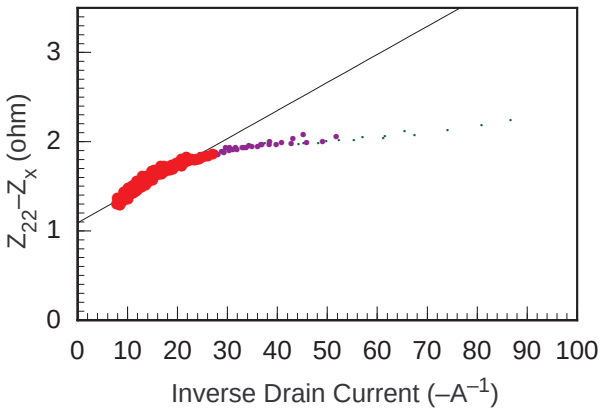

Fig. 3. A plot of drain-terminal impedance (20) using reduced sets of data with a reciprocal tolerance of 0.5 Ω, $|I_S| < 100$ mA. The large dots indicate $V_{DS} < -0.2$ V, and the medium dots indicate $V_{DS} < 0.1$ V, and small dots indicate $V_{DS} < 0.05$ V. The line is a least square fit to the large dots.

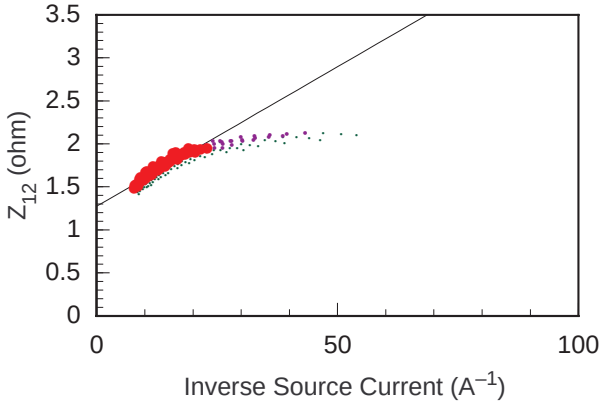

Fig. 4. A plot of source-terminal impedance (21) with reduced sets of data with $|I_D| < 100$ mA. The large dots indicate a reciprocal tolerance of 0.1 Ω, $V_{DS} > 0.2$ V, and the medium dots indicate a reciprocal tolerance of 0.1

$$Z_x = \frac{V_T}{I_D + I_G} + R_S \tag{21}$$

A plot of Z_x as a function of inverse source current has slope V_T and intercept R_S. Figure 4 shows that this plot approaches a straight line when the data set is reduced so that $V_{DS} \gg V_T$ and the reciprocal tolerance, $|Z_{12} - Z_{21}|$, is reduced. The line of best fit gives $V_T = 32.44$ mV and $R_S = 1.24$ Ω

Discussion

The new extraction technique is unique in that the data used is the difference between impedance measurements. This has the advantage of cancelling the intrinsic channel component. The slopes of the best-line fits used in the extraction closely agree that the thermal voltage, V_T, is around 32 mV (corresponding to an ideality factor of 1.24 at 300 K).

The new extraction has been implemented as a computer program that accepts arbitrary measured device data. The

TABLE I
EXTRACTED ACCESS RESISTANCES

Ω	Fukui [1]	This work
R_G	1.09	0.65
R_D	1.35	1.09
R_S	1.37	1.27

program uses a least-squares surface regression to determine the impedance matrices at each bias point. Then it isolates appropriate data sets and extracts the access resistances and thermal voltage using a linear least-square regression. The figures in this paper show typical data derived from the program.

Table I compares the resistances extracted from a 300μm MESFET using the new method with those extracted using the standard Fukui [1] method. The new method gives consistently lower values, suggestive of better exclusion of intrinsic channel component. This is typical of the many extractions with various types of devices.

CONCLUSION

A new access resistance extraction procedure has been presented, which suitable for implementation in automated test systems. The procedure uses impedance-difference data to eliminate the need to consider the intrinsic channel resistance. It is unique in that the characteristics are processed to find local small-signal impedances and impedance differences. Consistent results have been obtain from several devices, of which a typical example has been presented in this paper.

ACKNOWLEDGMENTS

This work was funded by Macquarie University and the Australian Research Council. The authors wish to thank M/A-COM, Inc. and Pacific Monolithics, Inc. for their support.

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